WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a first MOS transistor and a second MOS transistor integrated in the semiconductor substrate, wherein said second MOS transistor has a lower threshold voltage than said first MOS transistor and said first MOS transistor has a smaller channel length than said second MOS transistor; and

a punch-through stopper area that surrounds a source area and a drain area of said first MOS transistor and provides a punch-through voltage resistance between said source area and said drain area.

2. The semiconductor integrated circuit device according to Claim 1, wherein said first MOS transistor comprises a digital circuit device and said second MOS transistor comprises an analog circuit device.

3. The semiconductor integrated circuit device according to Claim 1, wherein a drain area of said second MOS transistor is surrounded by an offset drain area having a lower impurity concentration than the drain area of the second MOS transistor.

4. The semiconductor integrated circuit device according to Claim 3, further comprising a punch-through stopper area that surrounds a source area of said second MOS transistor and provides a punch-through voltage resistance between the source area of said second MOS transistor and said offset drain area.

5. The semiconductor integrated circuit device according to any of Claims 1 to 4, further comprising a bipolar transistor integrated in said semiconductor substrate.

6. The semiconductor integrated circuit device according to any of Claims 1 to 4, further comprising a diode integrated in said semiconductor substrate .

7. The semiconductor integrated circuit device according to any of Claims 1 to 4, further comprising a diffusion resistor integrated in said semiconductor substrate .

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8. The semiconductor integrated circuit device according to Claim 1, wherein said source area includes a source LDD area and said drain area includes a drain side LDD area, and wherein the punch-through stopper area had a pocket structure that enclosed the source side LDD area and the drain side LDD area.

9. A method for manufacturing a semiconductor integrated circuit device comprising a MOS transistor including a punch-through stopper area that offers a punch-through voltage resistance between a source area and a drain area, and a semiconductor element that does not require a punch-through stopper area in part or all of the area thereof, the MOS transistor and the semiconductor element being integrated on the same semiconductor substrate, the method comprising:

masking said semiconductor element;

forming said punch through stopper area using ion injection;

forming a gate polysilicon layer to be utilized in forming a gate electrode of said MOS transistor after the formation of said punch through stopper area.

10. A method for manufacturing a semiconductor integrated circuit device comprising a MOS transistor including a punch-through stopper area that offers a punch-through voltage resistance between a source area and a drain area, and a semiconductor element that does not require a punch-through stopper area in part or all of the area thereof, the MOS transistor and the semiconductor element being integrated on the same semiconductor substrate, the method being characterized in that:

forming a gate polysilicon layer that is to be utilized in forming a gate electrode of said MOS transistor; and

forming said punch-through stopper area using self-alignment-based ion injection method using said gate polysilicon as a mask.

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